WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor layer;

a plurality of semiconductor elements formed on said semiconductor layer;

an isolation film formed in a surface of said semiconductor layer, said semiconductor elements being electrically isolated from each other by said isolation film;

a PN junction portion formed by two semiconductor regions of different conductivity types in said semiconductor layer provided under said isolation film; and

a polysilicon film provided in a position opposed to a top of said PN junction portion with said isolation film interposed therebetween across said two semiconductor regions.

2. The semiconductor device according to claim 1, wherein said polysilicon film is formed in an upper portion of an outside of said isolation film, and

a formation width of said polysilicon film is set such that a length Lg from a position in said polysilicon film corresponding to a position of said PN junction portion to an end of said polysilicon film and

a thickness Tst of said isolation film satisfy an equation of $0.5\ Lg < Tst < 20\ Lg$.

3. The semiconductor device according to claim 2, wherein said semiconductor elements include a MOS transistor, and

a thickness of said polysilicon film is equal to that of a gate polysilicon film constituting a gate electrode of said MOS transistor.

4. The semiconductor device according to claim 2, wherein said semiconductor elements include a MOS transistor, and

a thickness of said polysilicon film is smaller than that of a gate polysilicon film constituting a gate electrode of said MOS transistor.

5. The semiconductor device according to claim 1, wherein said PN junction portion is extended along a provision pattern of said isolation film, and

said polysilicon film is provided along said PN junction portion.

6. The semiconductor device according to claim 1, wherein said polysilicon film is formed in said isolation film, and has a substantially uniform thickness across said two semiconductor regions.

7. The semiconductor device according to claim 6, wherein said isolation film has an upper oxide film and a lower oxide film which are provided in upper and lower portions of said polysilicon film, and

an oxide film spacer for covering side surfaces of said upper oxide film, said polysilicon film and said lower oxide film.

8. The semiconductor device according to claim 6, wherein said isolation film has an upper oxide film and a lower oxide film which are provided in upper and lower portions of said polysilicon film, and

an oxide film provided on a side surface of said polysilicon film.

9. The semiconductor device according to claim 6, wherein said polysilicon

film is connected to have a predetermined electric potential.

10. The semiconductor device according to claim 1, wherein said semiconductor device is an SOI semiconductor device formed on an SOI substrate including a silicon substrate, a buried oxide film provided on said silicon substrate and an SOI layer provided on said buried oxide film,

said semiconductor layer being said SOI layer.

11. A semiconductor device comprising:

a semiconductor layer;

a plurality of semiconductor elements formed on said semiconductor layer;

an isolation film provided in a surface of said semiconductor layer, said semiconductor elements being electrically isolated from each other by said isolation film; and

a PN junction portion formed by two semiconductor regions of different conductivity types in said semiconductor layer provided under said isolation film,

said isolation film including:

a nitride film provided in a position corresponding to a top of said PN junction portion and having a substantially uniform thickness across said two semiconductor regions; and

an upper oxide film and a lower oxide film which are provided in upper and lower portions of said nitride film.

12. The semiconductor device according to claim 11, wherein said semiconductor device is an SOI semiconductor device formed on an SOI substrate

including a silicon substrate, a buried oxide film provided on said silicon substrate and an SOI layer provided on said buried oxide film,

said semiconductor layer being said SOI layer.

13. A semiconductor device comprising:

an SOI substrate including a semiconductor substrate, a buried oxide film provided on said semiconductor substrate and an SOI layer provided on said buried oxide film;

a plurality of semiconductor elements formed on said SOI layer; and

an isolation film provided in a surface of said SOI layer, said semiconductor elements being electrically isolated from each other by said isolation film,

said isolation film including:

a complete trench reaching said buried oxide film penetrating through said SOI layer and a partial trench leaving a well region thereunder without penetrating through said SOI layer which are continuously provided;

an internal wall insulating film provided on internal walls of said complete trench and said partial trench;

an internal polysilicon film provided to fill in said complete trench and to be extended over a bottom face of said partial trench; and

an upper insulating film provided to cover said internal polysilicon film and surrounding said internal polysilicon film together with said internal insulating film, thereby electrically insulating said internal polysilicon film.

14. The semiconductor device according to claim 13, wherein said internal polysilicon film is restrictively provided in said partial trench so as not to get over said

internal wall insulating film formed on a side wall of said partial trench.

15. A semiconductor device comprising:

a semiconductor layer;

a plurality of semiconductor elements formed on said semiconductor layer;

an isolation film provided in a surface of said semiconductor layer, said semiconductor elements being electrically isolated from each other by said isolation film;

a PN junction portion formed by two semiconductor regions of different conductivity types in said semiconductor layer provided under said isolation film; and

a local crystal defect region provided along said PN junction under said isolation film on at least one of sides in said two semiconductor regions.

16. The semiconductor device according to claim 15, wherein said crystal defect region is a region in which an impurity of the same conductivity type as a conductivity type of said semiconductor region having said crystal defect region formed therein is introduced in a relatively high concentration.

17. The semiconductor device according to claim 15, wherein said crystal defect region is a region in which an impurity of a different conductivity type from said conductivity type of said semiconductor region having said crystal defect region formed therein is introduced in a relatively high concentration.

18. The semiconductor device according to claim 15, wherein said semiconductor device is an SOI semiconductor device formed on an SOI substrate including a silicon substrate, a buried oxide film provided on said silicon substrate and an

SOI layer provided on said buried oxide film,

said semiconductor layer being said SOI layer.

19. A semiconductor device comprising:

an SOI substrate including a semiconductor substrate, a buried oxide film provided on said semiconductor substrate and an SOI layer provided on said buried oxide film;

a plurality of semiconductor elements formed on said SOI layer;

an isolation film provided in a surface of said SOI layer, said semiconductor elements being electrically isolated from each other by said isolation film;

a PN junction portion formed by two semiconductor regions of different conductivity types in said SOI layer provided under said isolation film; and

a first polysilicon film buried to penetrate through the vicinity of said PN junction portion on at least one of sides in said two semiconductor regions.

20. The semiconductor device according to claim 19, wherein said semiconductor elements include a MOS transistor,

said MOS transistor having a source – drain region provided in a surface of said SOI layer, and

a second polysilicon film is further buried to penetrate through said source – drain region adjacent to said isolation film.

21. The semiconductor device according to claim 20, further comprising first and second local crystal defect regions provided in the vicinity of an interface between said silicon substrate and said buried oxide film under said first and second polysilicon

films.

22. A semiconductor device comprising:

a semiconductor layer;

a plurality of semiconductor elements formed on said semiconductor layer;

an isolation film formed in a surface of said semiconductor layer, said semiconductor elements being electrically isolated from each other by said isolation film;

a PN junction portion formed by two semiconductor regions of different conductivity types in said semiconductor layer provided under said isolation film: and

an upper nitride film provided in a position opposed to a top; of said PN junction portion with said isolation film interposed therebetween across said two semiconductor regions.

23. The semiconductor device according to claim 22, wherein said semiconductor elements include a MOS transistor,

said MOS transistor having a side wall spacer formed of a nitride film which is provided on side surfaces of a gate electrode and a gate insulating film, and

a thickness of said upper nitride film is substantially equal to that of said side wall spacer.

24. The semiconductor device according to claim 23, wherein said upper nitride film and said side wall spacer have a two – layered structure, and respective first layers and respective second layers have thicknesses substantially equal to each other.

25. The semiconductor device according to claim 22, wherein said

semiconductor device is an SOI semiconductor device formed on an SOI substrate including a silicon substrate, a buried oxide film provided on said silicon substrate and an SOI layer provided on said buried oxide film,

said semiconductor layer being said SOI layer.

26. A semiconductor device comprising:

a semiconductor layer;

a plurality of semiconductor elements formed on said semiconductor layer; and

an isolation film formed in a surface of said semiconductor layer, said semiconductor elements being electrically isolated from each other by said isolation film; and

a PN junction portion formed by two semiconductor regions of different conductivity types in said semiconductor layer provided under said isolation film,

said isolation film having a plurality of silicon islands therein,

said silicon islands being provided in a position corresponding to a top of said PN junction portion in said isolation film across said two semiconductor regions.

27. The semiconductor device according to claim 26, wherein said semiconductor device is an SOI semiconductor device formed on an SOI substrate including a silicon substrate, a buried oxide film provided on said silicon substrate and an SOI layer provided on said buried oxide film,

said semiconductor layer being said SOI layer.

28. A method of manufacturing a semiconductor device comprising:

a silicon semiconductor layer;

a plurality of semiconductor elements formed on said silicon semiconductor layer; and

an isolation film formed in a surface of said silicon semiconductor layer, said semiconductor elements being electrically isolated from each other by said isolation film, said method comprising the steps of:

(a) forming said semiconductor elements and then forming a metal layer to provide a silicide layer over a whole surface;

(b) carrying out a heat treatment to cause said metal layer to react to said silicon semiconductor layer, thereby forming a silicide layer; and

(c) removing an unreacted metal layer and a surface of said isolation film by a predetermined thickness after said heat treatment.

29. The method of manufacturing a semiconductor device according to claim 28, wherein said step (c) includes the steps of:

(c – 1) removing said unreacted metal layer by wet etching after said heat treatment; and

(c – 2) carrying out dry etching for removing said surface of said isolation film by said predetermined thickness after said step (c – 1),

said isolation film being formed of an oxide film,

said step (c – 2) including the step of:

using at least hydrofluoric acid as an etching agent,

said predetermined thickness being 2 to 50 nm.

30. The method of manufacturing a semiconductor device according to claim 29, further comprising, prior to said step (c – 2), the step of:

forming a mask setting at least a top of said isolation film to be an opening, said step (c – 2) being carried out by using said mask.